Simulating Moisture Distribution and its Impact on Delamination in a Microelectronics Package

A semiconductor package is a metal, plastic, glass, or ceramic casing containing one or more semiconductor electronic components. This casing provides protection for the semiconductor device and mechanical strength to support the leads and handling of the package. For economic reasons, many devices are encapsulated in an epoxy plastic, even though this material is hydrophilic and so absorbs moisture in a humid environment. The impact of moisture on interfacial delamination is two-fold. On one hand, it produces hygrostress, which increases the crack driving force, and on the other hand, it decreases the interface resistance to delamination propagation.

Obtaining accurate values of the distribution of moisture concentration in an Integrated Circuit (IC) package can be important. Hygrostresses are induced since polymers will expand with the absorption of moisture while other materials, such as metallic alloys, will neither absorb moisture nor expand. These stresses are in addition to the thermal stresses caused by the mis-match in thermal expansion between the materials. Moisture at a metal-polymer interface reduces its interfacial adhesion, and if a defect, a delamination, or a void is present, water vapor pressure can also add to the interfacial stress. With the knowledge of the moisture distribution within the package, the design of packages can be improved and the possibility of delamination can be reduced.

To achieve this objective, finite element simulation is very useful since analytical solutions are often limited to simple geometries and it is difficult to measure moisture concentration during physical tests. Many numerical schemes, such as the temperature-moisture analogy, normalization approach, and direct concentration approach, have been proposed to model moisture absorption and desorption. Some of the numerical schemes proposed might be capable of modeling physical observations more accurately but can be more involved than others.

In this numerical study, a plastic package (Plastic Quad Flat Pack, PQFP) with a small crack at the pad-encapsulant interface, is first subjected to moisture preconditioning (85°C/85%RH) and subsequently exposed to the solder reflow process, following the industry standard JEDEC J-STD-020C. Local moisture concentration and fracture mechanics parameters at the interface crack—energy release rate (ERR) and mode mixity—are determined using Abaqus. Figure 1 shows the moisture concentration in the package obtained from the simulations. The thickness of the package and the assumptions made in the numerical model greatly influenced the local moisture concentration during solder reflow. Dependence of C_{sat} on temperature is commonly observed in materials at elevated temperatures. In such cases, although the moisture content in the atmosphere is low, the local moisture concentration can increase during solder reflow. Figure 2 illustrates examples of the described phenomenon. When a package is thick, for instance in the case of "Thickness" and "3/4 Thickness," moisture concentration at the crack tip continues to increase during the entire solder reflow process, whereas for a thinner package, moisture concentration reaches a peak at around five minutes and decreases thereafter. ERR and phase angle arising from a combination of moisture, vapor pressure, and temperature factors are then calculated.

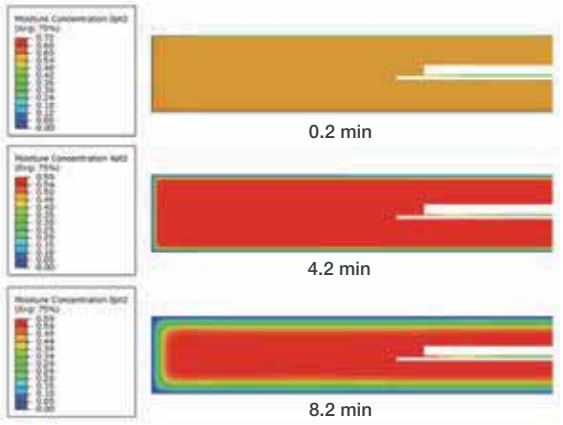

Figure 1. Moisture distribution during solder reflow.

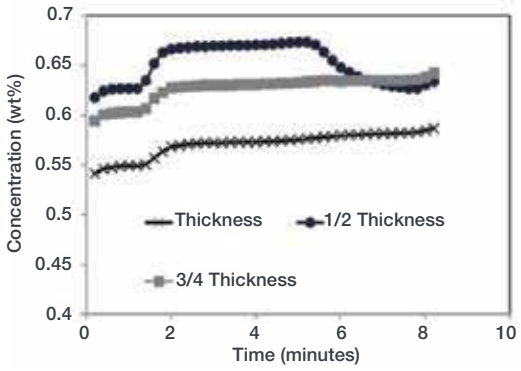

Figure 2. Effect of package thickness on moisture concentration on the crack tip.

It is observed that a thicker package leads to higher ERR and for all the cases, ERR reaches a maximum in the vicinity of peak solder reflow (around 5-6 minutes) primarily attributed to the increase in mismatch of thermal expansion with elevated temperature. Higher moisture concentration at the interface will lead to increased degradation of the interface. With the combined effects of reduction in interfacial toughness and increase of thermal ERR due to elevated temperature, the risk of delamination during solder reflow increases significantly especially at peak solder reflow temperature.

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