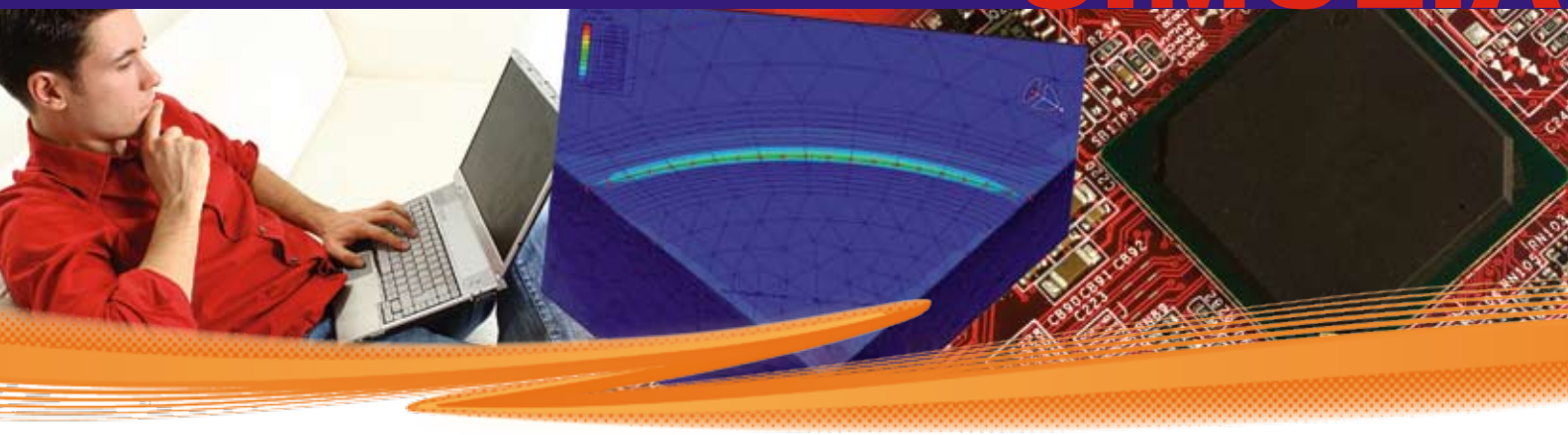

Advanced Micro Devices uses Abaqus FEA to Improve the Reliability of Chip Packaging

Developed in the 1960s by IBM for use in mainframe computers, flip-chips are now used in all kinds of electronic devices including watches, smart cards, RFID tags, and cellular telephones. The chips are mounted face-down, or "flipped", directly onto a substrate, circuit board, or carrier. They make an electrical connection through precisely positioned bumps or tiny spheres of conductive material, which allow heat to dissipate from the chip, act as a spacer between the chip and the board or substrate circuits, and provide mechanical support for the chip.

"In flip-chip packages, the mismatch in coefficients of thermal expansion (CTE) of the various layers induces stresses that can result in delamination," says Zhen Zhang, Senior Packaging Engineer, at Advanced Micro Devices (AMD), a global supplier of integrated circuits, based in Sunnyvale, CA. The underfill is a layer of adhesive between the chip and substrate that ensures electrical contact is maintained by adding mechanical strength to the assembly and protecting the contact points from moisture.

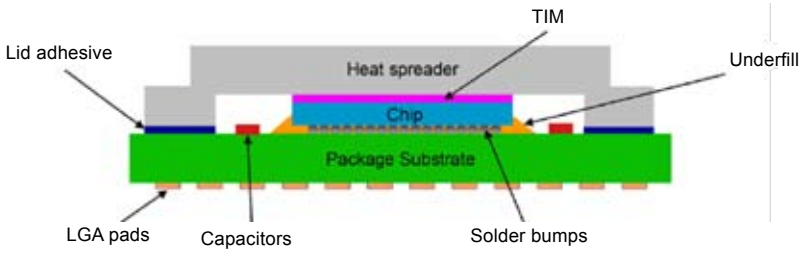

Figure 1. Schematic of generic flip-chip. The flip-chip faces down and is typically attached via solder bumps to the printed package substrate or circuit board. The underfill layer locks the die, or chip, to the substrate layer, protecting the bumps and improving durability.

To help predict and prevent delamination during cyclic thermal loading, AMD is using Abaqus finite element analysis (FEA) software from SIMULIA, the Dassault Systèmes brand for realistic simulation, to analyze the effect of underfill variables including the material modulus, CTE, and the dimensions of the underfill layer (fillet height). "We chose Abaqus because of its powerful fracture mechanics capabilities," says Zhang. "In addition, it has other features—such as contact mechanics, global-local submodeling routines, surface-to-surface tie constraints, a variety of partition and meshing tools, and parametric GUI and Python scripting for high productivity."

The Abaqus simulation results helped the AMD engineers to determine that among other factors: the underfill layer material should have a low CTE; the fillet height should be increased; and the glass transition temperature of the material should be as low as possible. "We have optimized solder joints, the contact reliability of the package bottom with the socket, and various package sizes for both single-chip and multi-chip modules—all using Abaqus." In this case, Zhang adds, "The analysis provided reliability data for all flip-chips in which underfill is incorporated—from package to board level, and from assembly to service conditions."

SIMULIA

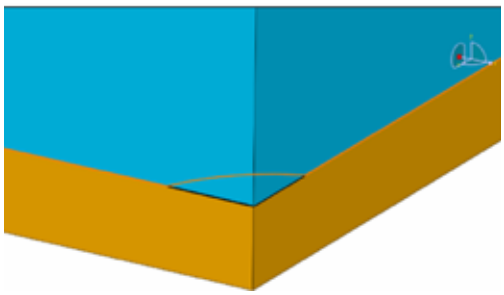

Figure 2b. A model of a pre-existing crack (center). The upper part of the model (blue) is silicon die, and the lower part (yellow-brown) is the underfill. This crack replicates a situation in which a micro-crack is initiated from the die corner, or an existing flaw due to an unclean surface.

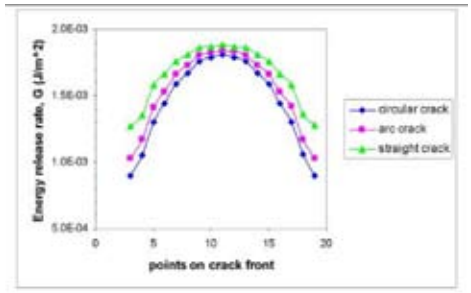

Figure 3. FEA analysis showing the stress field at the crack front.

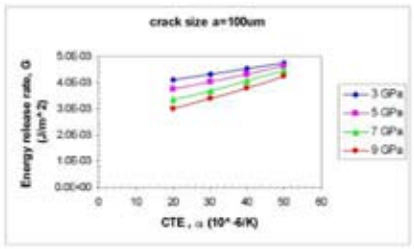

Figure 4a. Chart of the energy release rate vs. crack front location under thermal excursion loading ΔT= 1oC.

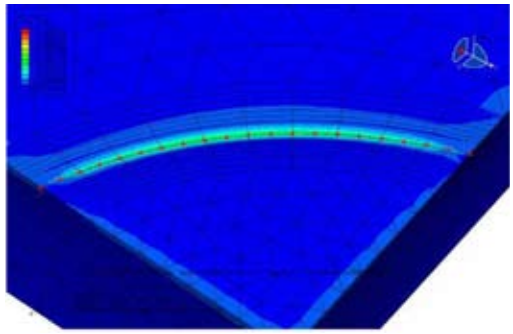

Figure 4c. Energy release rate plotted as a function of underfill CTE for different modulus with fixed crack size (100um) and ΔT= 1oC. The results validate the general recommendation of lower-CTE underfill.

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