Prediction of Crack Propagation in Stacked IC Packages

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Abstract

Because high performance and better reliability as well as lower cost are demanded for most of electronic applications, three-dimensional (3D) IC packaging technologies are presently discussed to achieve these objects. Even though the miniaturization of system scaling, the low power consumption and the better electrical performance can be performed by 3D IC packaging technologies, thermo-mechanical problems occur as well. Due to the reason of stacking chips, the heat dissipation, high thermal resistances, induced thermo-mechanical stresses, interfacial delamination, crack propagation and so on are presented and always caused failures in 3D IC devices. These problems are becoming significant reliability concerns in electronic industry. Among these reliability concerns, the problem of crack propagation is the mostly common failure type when larger stresses are resulted in 3D stacked IC packages. Moreover, by the use of spacers, the inner thermal resistance can be effectively reduced and helpful to uniform the chip temperature, but larger stresses of TSV (through-silicon-via) and chip structures are occurred in stacked IC packages. For the purpose of realizing thermal stress distributions and the phenomenon of crack propagation in stacked IC packages, the three dimensional finite element analysis (FEA) modeling as well as eXtended Finite Element Method (XFEM) has been employed by Abaqus. Through the modeling result, it is found that the crack is started to be propagated at TSV structure while larger maximum principal stresses are carried out. To investigate effects of material properties in stacked IC packages, several materials of isolation walls are selected as design factors and the maximum von Mises stress in copper TSV and chips are chosen as the response to be optimized. By using the FEA modeling results, most desirable values of material properties in stacked IC packages and their corresponding results in smaller von Mises stress in Cu TSV and chips can be illustrated. By using the optimized material, it is found that there is no crack propagation in stacked IC packages. These results will be effective design guidelines to engineers for prevent the propagation of cracks in stacked IC packages.

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